IN THE SPECIFICATION:

Page 6, last paragraph on page.

The comparison circuit 10 uses the bias voltage that controls the current source 2 to compare the current output by the current source 2 with a reference value, and outputs a control signal according to the comparison result. The output current adjustment transistor 11 adjusts the external current flow from the DP terminal or the DM terminal by shunting part of the output current of the current source 2 to ground, based on the value of the control signal output by the comparison circuit 10~~n~~. When the OE signal indicates the output disabled state, in which no output current may flow from the DP terminal or the DM terminal, both of the switches 3 and 4 are turned off, and the voltage at their common node N is substantially equal to the power supply voltage (VDD). When the differential current driver transitions from this state to the output enabled state, one of the switches 3 and 4 turns on responsive to the data signal, and the voltage at the common node N abruptly decreases. The bias voltage at the gate of the current source 2 also decreases due to gate-to-drain capacitive coupling in the current source 2. As a result, the output current of the current source 2 increases. For this reason, without current adjustment, more current than required would be output from the DP terminal or the DM terminal, until the bias voltage returned to its normal level.

Page 8, 1st full paragraph on page.

Since the conductivity of the current source 2 and the conductivity of PMOS transistor 23 are controlled by the same bias signal, the drain current of PMOS transistor 23 mirrors the output current of the current source 2, being proportional to the output current of the current source 2. The dimensions of the current source 2 and PMOS transistor 23 are selected so that the drain current of PMOS transistor 23 is less than the output current of the current source 2.